PROJECT TITLE:	Strategic Substrate Development for Coated Conductors
ORGANIZATION:	Oak Ridge National Laboratory
PRESENTERS:	Amit Goyal (ORNL) and M. Parans Paranthaman (ORNL)
FY 2008 FUNDING:	$ 425 K (DOE to ORNL)

Overall Project Purpose and Objectives:

The objective of this project is to conduct fundamental research in the broad areas of substrate or template and buffer layer development. The results of this project provide new insights in these areas and suggest methods to improve substrate and buffer fabrication at partner companies such as American Superconductor and SuperPower. The overall purpose of this project is to enable potentially low-cost, high throughput, high yield, manufacturing processes for substrate and buffer fabrication, and to gain fundamental understanding of the growth of buffer layers for both RABiTS and IBAD-MgO templates. This understanding is critical to the development of a reliable, robust, long-length manufacturing process of 2G wires.

FY 2008 Plans were:

1. Understand current limiting mechanisms for epitaxial HTS films on RABiTS to guide further improvements in substrate fabrication
2. Continue to develop substrate technology for the RABiTS process – develop powder metallurgy based coils and develop processes to increase strength, reduce magnetism, or enhanced texture in the substrates
3. Continue development of simplified buffer architectures leading to improved RABiTS/IBAD-MgO template performance and/or reduced manufacturing cost
4. Further develop MOD based seed layers to sustain an I_c of 250 A/cm
5. Develop a low-aspect ratio, "round" template for epitaxial growth of HTS for applications requiring low AC losses
6. Transfer the knowledge learned from the substrate and buffer development research to our industry partners

2008 Approach and Results:

We have continued to investigate methods to achieve biaxial texture in substrates which are mechanically strong and have reduced magnetism. In the area of buffer layer development, the emphasis areas included – development of buffers which improve the texture compared to the substrate, development of multifunctional buffer layers, reduction in the number of buffer layers and development of more robust buffers.

Specific results and accomplishments in FY2008 include:

- Studied grain boundary networks in YBCO films on RABiTS and correlated results with measurements on $SrTiO_3$ bicrystals in collaboration with Univ. of Augsburg – results show which Gb's limit J_c
- In collaboration with Ametek and AMSC, improved the powder metallurgy coil making process to result in well textured substrates
- Improved texture of substrates fabricated from vacuum casting derived coils

- Studied the effect of humidity during coating on the growth of solution based La_3NbO_7 (LNO) buffers – results show RH 40-60% during coating improves the LNO texture compared to the underlying NiW substrate
- Identified process conditions to grow solution based La_3TaO_7 (LTO) buffers directly on Ni5W substrates with improved texture
- Improved process conditions to result in a J_c of over 3 MA/cm^2 on simplified RABiTS buffer architecture of NiW/Modified LZO/PVD CeO_2
- Developed process conditions to grow solution based CeO_2 cap layers on slot-die coated LZO buffers
- Developed process conditions to grow epitaxial LMO using rf-sputtering directly on IBAD-MgO and demonstrated the growth of thick YBCO films with similar performance on both with/without homoepitaxial MgO layers
- Developed a new and promising process to fabricate long –lengths of low-aspect ratio or "round" templates for epitaxial growth of HTS conductors

2009 Plans and Expectations:

U.S. HTS wire manufacturers are now in a position to produce reasonable quality coated conductors in "pilot-scale" mode. Presently, up to 3-5 buffer layers are used in the standard RABiTS/IBAD-MgO architecture of 2G wires. To reduce cost and complexity, as well as associated mechanical and reliability concerns, it is highly desirable to reduce the number of buffer layers. This can be accomplished by utilizing multi-functional materials that can combine the tasks of two buffers into one. Development of robust buffer stacks on these buffers is also needed.

FY 2009 Plans include:

1. Continue to further develop substrate technology for the RABiTS process – develop powder metallurgy based coils and develop processes to increase strength, reduce magnetism, or enhanced texture in the substrates
2. Continue development of simplified buffer architectures leading to improved RABiTS/IBAD-MgO template performance and/or reduced manufacturing cost
3. Further develop MOD based solution layers and transfer the technology to slot-die coating efforts in the ORNL-AMSC CRADA
4. Further develop the new and promising process to fabricate long –lengths of low-aspect ratio or "round" templates for epitaxial growth of HTS conductors
5. Transfer the knowledge learned from the substrate and buffer development research to our industry partners

Technology Transfer, Collaboration, Partnerships:

Close collaboration and interaction with American Superconductor Corporation (AMSC) and SuperPower has resulted in significant advancement in process understanding and subsequently in the development of a robust manufacturing process at AMSC and SuperPower. Several publications and presentations have resulted from this work. In recognition of the importance of the ORNL LMO technology, ORNL team has won a National Federal Laboratory Consortia (FLC) award for 2008. A very close interaction with AMSC was prevalent for the entire FY year. Significant assistance was provided to AMSC which resulted in significant improvements in the quality of their metal templates and buffers in their production process.